UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/783,886 | 02/20/2004 | Om P. Agrawal | M-15311 US | 6972 |

7590 09/02/2005

Greg J. Michelson
MacPHERSON KWOK CHEN & HEID LLP
Suite 226
1762 Technology Drive
San Jose, CA 95110

| EXAMINER | |
|---|---|
| LE, DON P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/783,886 | AGRAWAL ET AL. | |
| | Examiner | Art Unit | |
| | Don P. Le | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-35 are rejected under 35 U.S.C. 102(a) as being anticipated by Fox et al. (US 6,851,047).

3. With respect to claim 1 figure 2 of Fox teaches a programmable logic device comprising:

volatile memory (configuration memory in 201) adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory (203) adapted to store data which is transferable to the volatile memory to configure the programmable logic device;

a first data port (JTAG) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory; and

a second data port (CPU 206) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

4. With respect to claims 2, 16 and 29, the apparatus of Fox teaches control logic (figure 2 shows control circuit system bus 205) adapted to transfer the data from the non-volatile memory to the volatile memory to configure the programmable logic device.

5. With respect to claims 3 and 17, the apparatus of Fox teaches core logic adapted to be configured by the configuration data stored in the volatile memory (see column 1, lines 35-40).

6. With respect to claim 4, apparatus of Fox teaches the volatile memory comprises static random access memory (Xilinx FPGA uses RAM for configuration memory) and the non-volatile memory comprises flash memory (EEPROM, see column 4, line 10).

7. With respect to claims 6, 28 and 30, Fox teaches the first data port is a JTAG port (102) and the second data port is a CPU port (206).

8. With respect to claims 7 and 15, the apparatus of Fox supports an IEEE 1149.1 standard, with the external data transferred to the non-volatile memory and/or the volatile memory via an IEEE 1532 programming mode or to the non-volatile memory via a background programming mode.

9. With respect to claim 8, the apparatus of Fox teaches the external data is transferred through the second data port to the volatile memory via a system configuration mode, to the non-volatile memory directly, and/or to the non-volatile memory via a background programming mode (see figure 2).

10. With respect to claim 9, the apparatus of Fox teaches the programmable logic device further supports reading back of the configuration data stored in the volatile memory and/or the data stored in the non-volatile memory for verification (see figure 3B, 321, has to read data in order to check sum).

11. With respect to claims 10 and 27, the apparatus of Fox teaches the programmable logic device further supports the reading back while the programmable logic device performs its intended function based on the configuration data stored by the volatile memory (see column 3, lines 25-35, configuration data in memory can be checked while logic is operating).

12. With respect to claim 11, the apparatus of Fox teaches the programmable logic device supports transfer of the external data the non-volatile memory while the programmable logic device is operable to perform its intended logic functions (same reasoning as claim 10, see column 3, lines 25-35).

13. With respect to claim 12, figures 1 and 2 of Fox teaches a programmable logic device, comprising:

static random access memory (configuration memory in 201) adapted to configure the programmable device for its intended function based on configuration data stored by the static random access memory;

flash memory (203) adapted to store data which is transferable to the static random access memory to configure the programmable device;

a JTAG port (102, figure 1) adapted to receive external data for transfer into either the static random access memory or the flash memory;

a CPU port (206) adapted to receive external data for transfer into either the static random access memory or the flash memory; and

means (207) for transferring the external data received by the JTAG port or the CPU port to the static random access memory or the flash memory.

14. With respect to claim 13, figure 2 of Fox teaches the means (207, see column 6) comprises:

a background mode adapted to transfer the external data from the JTAG port to the flash memory or transfer the external data from the CPU port to the flash memory;

a programming mode adapted to transfer the external data from the JTAG port to the flash memory and/or to the static random access memory; and

a system configuration mode adapted to transfer the external data from the CPU port to the static random access memory.

15. With respect to claim 14, the apparatus of Fox teaches the background mode and the programming mode are further adapted to support readback of data stored in the flash memory and the static random access memory (see column 6, lines 45-51).

16. With respect to claims 18-24 and 31-35, the methods therein are inherent given the apparatus of Fox as shown in the above rejections.

17. With respect to claim 25, figures 1 and 2 of Fox teaches a programmable logic device comprising:

volatile memory (configuration memory in 201) adapted to configure the programmable logic device (201) for its intended function based on configuration data stored by the volatile memory;

non-volatile memory (203) adapted to store data which is transferable to the volatile memory to configure the programmable logic device; and

a CPU port (port connected to 206) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

18. With respect to claim 26, the apparatus of Fox teaches the volatile memory comprises static random access memory and the non-volatile memory comprises flash memory.

## Claims 1-5 are rejected again using different elements for the purpose of rejecting claim 5.

19. With respect to claim 1, figures 1 and 2 of Fox teaches a programmable logic device comprising:

volatile memory (configuration memory in 201) adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory (103, figure 1) adapted to store data which is transferable to the volatile memory to configure the programmable logic device;

a first data port (JTAG) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory; and

a second data port (CPU 206) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

20. With respect to claim 5Fox teaches the non-volatile memory store security bits (see column 5, lines 24, 25).

20. Claim1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsui et al. (6,828,823).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the

inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

21. Claims 1 and 2 are rejected under 35 U.S.C. 102(a) as being anticipated by Tsui et al (US 6,828,823).

22. With respect to claim 1, figures 1-3 of Tsui teach a programmable logic device comprising:

volatile memory (104) adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory (102) adapted to store data which is transferable to the volatile memory to configure the programmable logic device;

a first data port (JTAG connected to 206 of figure 2) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory; and

a second data port (JTAG connected to 210 of figure 2) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

23. With respect to claim 2, figure 2 of Tsui discloses control logic (figure 2 shows control circuit to transfer signal from 202 to 204) adapted to transfer the data from the non-volatile memory to the volatile memory to configure the programmable logic device.

24. With respect to claim 3, the apparatus of Tsui teaches core logic adapted to be configured by the configuration data stored in the volatile memory (see column 1, lines 40-55).

25. With respect to claim 4, figures 1-3 of Tsui teach the volatile memory comprises static random access memory (104) and the non-volatile memory comprises flash memory (EEPROM).

26. With respect to claim 5, the apparatus of Tsui teaches the non-volatile memory EEPROM) is further adapted to store security bits that can be set to prevent unauthorized reading of the data from the programmable logic device (see column 3, lines 35-45).

27. With respect to claim 6, figure 2 of Tsui teaches the first data port is a JTAG port (206) and the second data port is a CPU port (210).

28. With respect to claim 7, the apparatus of Tsui supports an IEEE 1149.1 standard, with the external data transferred to the non-volatile memory and/or the volatile memory via an IEEE 1532 programming mode or to the non-volatile memory via a background programming mode.

29. With respect to claim 8, the apparatus of Tsui teaches the external data is transferred through the second data port to the volatile memory via a system configuration mode, to the non-volatile memory directly, and/or to the non-volatile memory via a background programming mode (see figure 2).

30. With respect to claim 9, the apparatus of Tsui teaches the programmable logic device further supports reading back of the configuration data stored in the volatile memory and/or the data stored in the non-volatile memory for verification.

31. With respect to claims 10 and 27, the apparatus of Fox teaches the programmable logic device further supports the reading back while the programmable logic device performs its intended function based on the configuration data stored by the volatile memory (see table 1).

32. With respect to claim 11, the apparatus of Fox teaches the programmable logic device supports transfer of the external data the non-volatile memory while the programmable logic device is operable to perform its intended logic functions (see table 1).

33. With respect to claim 12, figures 1 and 2 of Fox teaches a programmable logic device, comprising:

static random access memory (104) adapted to configure the programmable device for its intended function based on configuration data stored by the static random access memory;

flash memory (102) adapted to store data which is transferable to the static random access memory to configure the programmable device;

a JTAG port (302) adapted to receive external data for transfer into either the static random access memory or the flash memory;

a CPU port (304) adapted to receive external data for transfer into either the static random access memory or the flash memory; and

means (circuitry 310, 312, 314) for transferring the external data received by the JTAG port or the CPU port to the static random access memory or the flash memory.

34. With respect to claim 13, apparatus of Tsui teaches the means (310, 312, 314) comprises:

a background mode adapted to transfer the external data from the JTAG port to the flash memory or transfer the external data from the CPU port to the flash memory;

a programming mode adapted to transfer the external data from the JTAG port to the flash memory and/or to the static random access memory; and

a system configuration mode adapted to transfer the external data from the CPU port to the static random access memory.

35. With respect to claim 14, the apparatus of Tsui teaches the background mode and the programming mode are further adapted to support readback of data stored in the flash memory and the static random access memory.

36. With respect to claims 18-24 and 31-35, the methods therein are inherent given the apparatus of Tsui as shown in the above rejections.

37. With respect to claim 25, figures 1-4 of Tsui teaches a programmable logic device comprising:

volatile memory (104) adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory (102) adapted to store data which is transferable to the volatile memory to configure the programmable logic device; and

a CPU port (304) adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

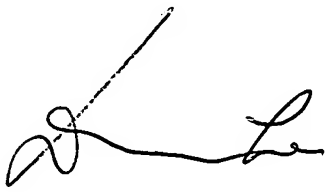
38. With respect to claim 26, the apparatus of Tsui teaches the volatile memory comprises static random access memory and the non-volatile memory comprises flash memory.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/29/2005



DON LE
PRIMARY EXAMINER